



e-ISSN: 2319-8753 | p-ISSN: 2347-6710

IJRSET

International Journal of Innovative Research in
SCIENCE | ENGINEERING | TECHNOLOGY

INTERNATIONAL JOURNAL OF INNOVATIVE RESEARCH

IN SCIENCE | ENGINEERING | TECHNOLOGY

Volume 12, Issue 6, June 2023

ISSN INTERNATIONAL
STANDARD
SERIAL
NUMBER
INDIA

Impact Factor: 8.423

 9940 572 462

 6381 907 438

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Performance Analysis of 5-Level Diode Clamp Single Phase Inverter

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ABSTRACT: Multilevel inverters (MLIs) have been widely accepted as a potential solution for high-efficiency electric power-electronic conversion systems by both research and industry community. The inherent features of MLIs like reduced dv/dt , high-quality output waveform, lower switching frequency, etc., are the key reasons for the usage of MLIs in a variety of fields including motor drives, renewable energy sources integration, locomotives, to name a few. Renewable energy sources use to generate green energy for reduce environment pollution problem. In this paper build a PV system that is transmit a power to the grid. A grid connected photovoltaic system is becoming increasingly important for the solution in renewable energy. Various types of inverter have been proposed for PV grid connected application such as multilevel inverters, current source inverter, voltage source inverter and etc. In this block diagram shows PV to grid connected system. This work processed in two stage where, stage one is the DC-DC boost converter with MPPT (Maximum power point) tracking and second stage is the five-level inverter. For this stage proposed a new five-level inverter topology which is reduce the switched count and other parameters. After this stage levelled output passes through designed LCL filter which gives AC output and connected to grid. Its achieves a minimum value of the THD i.e., 0.46% that is good enough to use for the grid and also can be used for the different load applications.

KEYWORDS: Multi-level Inverter, 13-level, PWM, Boost Factor

I. INTRODUCTION

In modern technology, power electronics and processor plays a vital role in the field of motor control, light control, heat control, power supplies, vehicle system, HVDC, FACTS and renewable applications. The philosophy focuses on preserving the energy and meeting the power demand accurately and the power modulator pertaining to inverter / converter technology fulfills the requirements and this attracts the researchers to explore in the inverter field. The above-mentioned applications work in the range of medium power, high power at a higher voltage. With the help of semiconductor device technology, power converters are to be designed with higher operating voltage. As a single device fails to support such high voltages, a number of devices need to connect in series to meet the voltage rating. Another challenge in the industrial sector is the requirement and maintenance of the sinusoidal power supply with variable voltage and frequency. The above demerits are overcome by the introduction of Inverters. The series connected switches in the inverters and through control mechanism, the voltage stress with respect to high voltage rating is shared among the series switches and also the losses are minimized. Due to advantage of minimum losses, inverters is also used for medium voltage applications. The classical square wave inverter operating at higher voltage introduces the dominant harmonics, thereby the performance on the load side and on the front end of the inverter has a large impact and the performance is affected. Though the solution is sought through the passive filters, the loss are increased and occupies more space. The alternative path is provided by Multilevel Inverters (MLI) [1, 2]. MLI generates sinusoidal voltage waveform in the form voltage steps through switching sequence. The other advantages of MLI are reduced electromagnetic interference, reduced current distortion, good quality voltage waveform, good current waveform. The basic types of MLI are neutral point clamped MLI, flying capacitor MLI and cascaded H- bridge MLI. To synthesize nearly sinusoidal voltage, higher number of levels needs to be generated with the help of more number of switches, more number of sources and more number of gate drivers [3, 4]. Due to this, the efficiency decreases as more number of switches is utilized in the conduction path.

II. MULTI LEVEL INVERTER TOPOLOGIES

The conventional single phase inverter suffers from a drawback of higher THD. Hence, it is not suited for grid connected applications. MLIs have many advantages for medium and high power systems as they synthesis a higher output voltage rating of each switching device. Stepped output voltage allows a reduction in harmonic content of

voltage and current waveforms, switching frequency and semiconductor voltage level. The presented merits make MLIS appropriate for RE applications. The best well known multilevel inverter topologies are diode clamped, flying capacitor and cascaded MLIS [5, 6].

2.1 Diode Clamped Multilevel Inverter

Concept of the diode clamped topology was proposed by Nabae et al 1981. This topology has found wide acceptance for its capability of higher voltages and high efficiency operation. A phase leg of a three-level diode clamped inverter is shown in Figure 1(a). It consists of two pairs of switches and diodes. Each switching pairs works in complementary mode and the diodes are used to provide access to mid-point voltage. The DC bus voltage is split into three voltage levels by using two series connection of DC capacitors, C1 and C2. Each capacitor is supposed to have an equal DC voltage and each voltage stress will be limited to one capacitor level through clamping diodes (DC1 and DC2). If assumed that total DC link voltage is V_{dc} and mid-point is regulated to half of the DC link voltage, the voltage across each capacitor is $V_{dc}/2$ ($V_{C1} = V_{C2} = V_{dc}/2$). Based on the structure of the diode clamped inverter, there are three different possible switching states which apply the staircase voltage on output voltage relating to DC link capacitor voltage rate. Switching states of the three level inverter are summarized in Table 1.

To study the effect of the number of output voltage levels in diode clamped topology, Figure 1(b) shows a phase leg of a four-level inverter. If converter works in balance condition, DC link voltage split into three different values by the series capacitor ($V_{C1} = V_{C2} = V_{C3} = V_{dc}/3$).

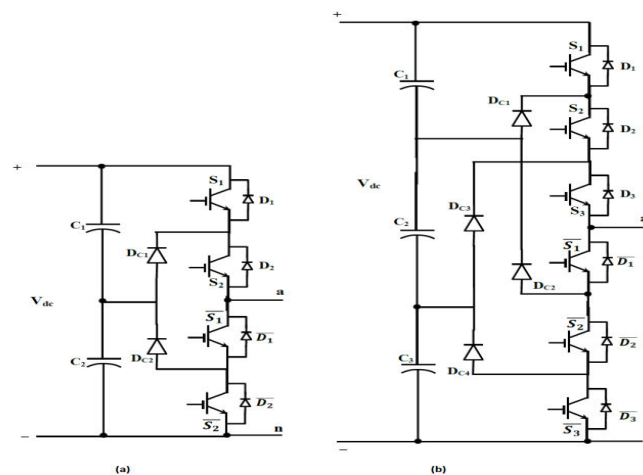


Figure 1: One leg of diode clamped inverter (a) three-level (b) four level

Table 1: Switching states in one leg of the three-level diode clamped inverter

S ₁	S ₂	Leg Voltage (V _{an})
ON	ON	V_{dc}
OFF	ON	$V_{dc}/2$
OFF	OFF	0

III. PROPOSED METHODOLOGY

Representation of this work using block diagram which is shown in figure 2

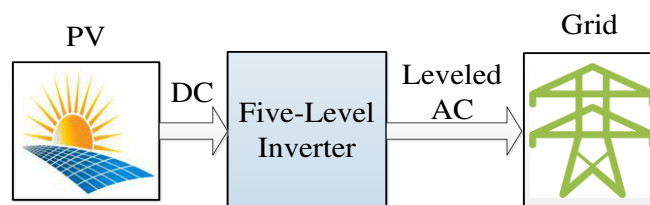


Figure 2: Representation of PV energy to grid connected system

Designing of 5-Level Inverter

In this work proposed a novel 5 level inverter which is suitable to connect PV and transmit a power to the grid. Proposed inverter generates a five level at the output of the inverter as V_{dc} , $V_{dc}/2$, 0 , $-V_{dc}/2$, V_{dc} . Proposed topology is represented in figure 3. This topology has 8 unidirectional switches and 4 diodes and it have 2 capacitors as a dc-bus capacitor which is connected after the first stage which is DC-DC boost converter. Levelled voltage as a five-level voltage occurs at the output of the inverter.

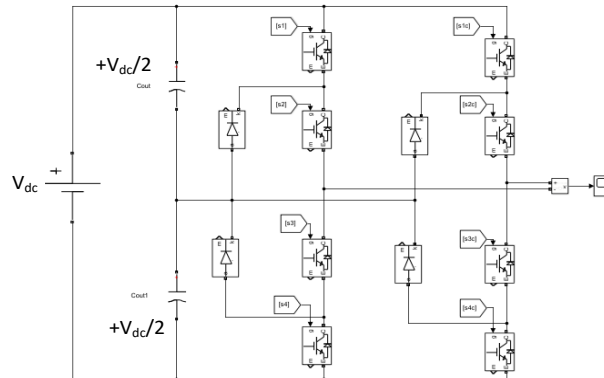


Figure 3: Proposed five level topologies

+V_{dc} level

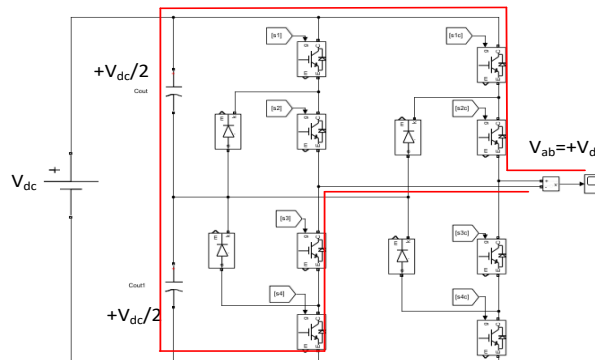


Figure 4: +V_{dc} Level

By turning ON switch S3, S4, S1c and S2c and other switch OFF, capacitors C1 and C2 are connected in series through the load and it gives +V_{dc} voltage at the output of inverter. This stage specified in Figure 4.

+V_{dc}/2 Level

By turning ON switch S2, S3c and S4c and other switch OFF, capacitors C2 is connected in series through the load and C1 is by passed and it gives +V_{dc}/2 voltage at the output of inverter. This stage specified in Figure 5.

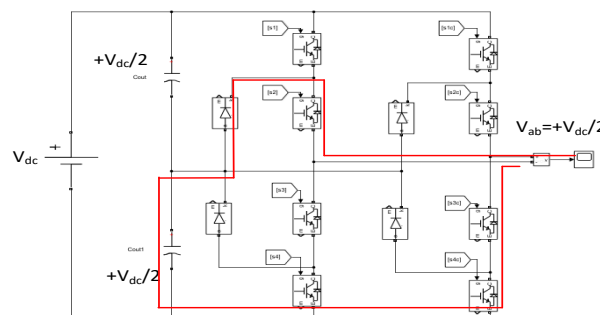


Figure 5: +V_{dc}/2 Level

0 Level

By turning ON switch S3, S4, S3c and S4c and other switch OFF, capacitors C1 and C2 are by passed and it gives 0 voltage at the output of inverter. This stage specified in Figure 6.

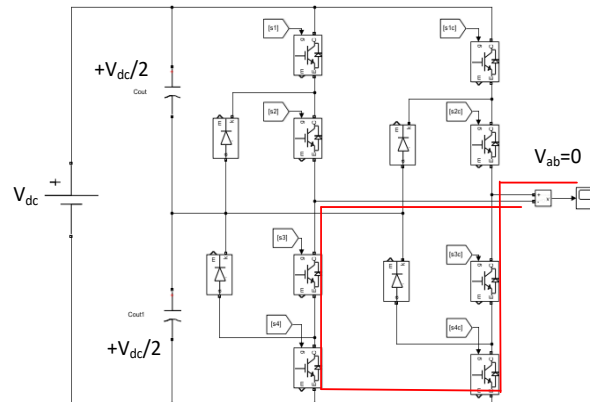


Figure 6: 0 Level

-Vdc/2 Level

By turning ON switch S1, S2 and S2c and other switch OFF, capacitors C1 is connected in series through the load and C2 is by passed and it gives -Vdc/2 voltage at the output of inverter. This stage specified in Figure 7.

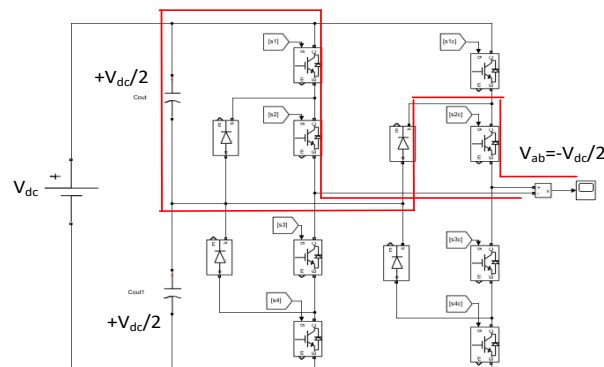


Figure 7: -Vdc/2 Level

-Vdc Level

By turning ON switch S1, S2, S3c and S4c and other switch OFF, capacitors C1 and C2 are connected in series through the load and it gives -Vdc voltage at the output of inverter. This stage specified in Figure 8.

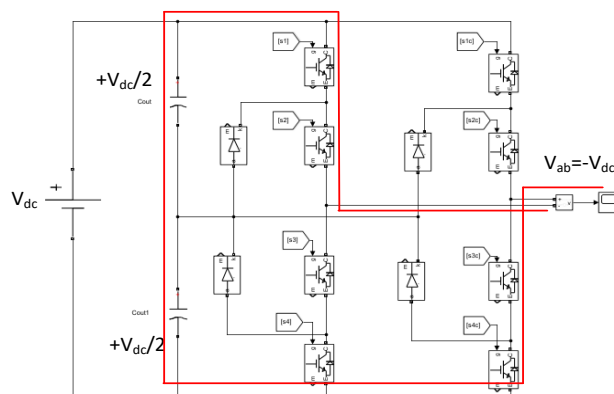


Figure 8: -Vdc Level



Generation of PWM signal for the proposed converter is described in Table 2.

Table 2: Switching States of the Proposed 5-Level Converter

State	Voltage Level	S1	S2	S3	S4	S1c	S2c	S3c	S4c
1	+Vdc	0	0	1	1	1	1	0	0
2	+Vdc/2	0	1	0	0	0	0	1	1
3	0	0	0	1	1	0	0	1	1
4	-Vdc/2	1	1	0	0	0	1	0	0
5	-Vdc	1	1	0	0	0	0	1	1

IV. SIMULATION RESULT

Figure 9 shows the dynamic response of the proposed multilevel inverter. In this intense the inductive load changes from 100Ohm 200mH to 50Ohm 100mH at the time of 0.5sec. It can be clearly seen that the output voltage has not change at this time but output current has been doubled at this point. Its changes from 1.5A to the 3A after doing half of the inductive load.

Figure 10 shows the dynamic response of the proposed multilevel inverter. In this intense the inductive load change from 100Ohm 100mH to pure resistive load 50Ohm at the time of 0.5sec. It can be clearly seen that the output voltage has not change at this time but output current has been doubled at this point. Its changes from 1.8A inductive current to the 4A resistive current after doing change the load.

Figure 11 shows the Total harmonic profile (THD) of the output current. Its achieves a minimum value of the THD i.e., 0.46% that is good enough to use for the grid and also can be used for the different load applications. Figure 11 shows the PWM pulses across the switches.

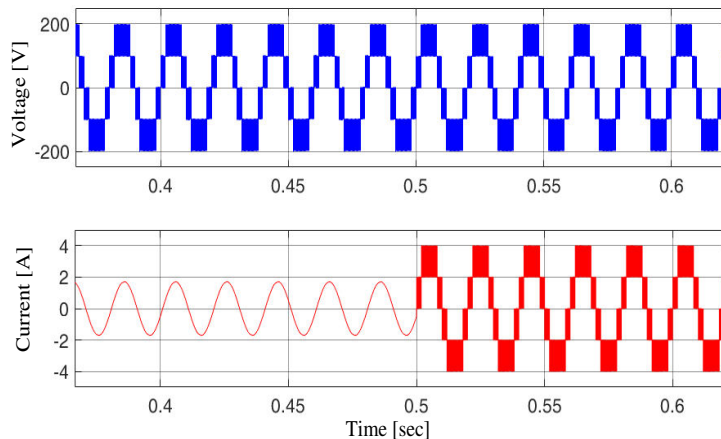


Figure 9: Output voltage and current with inductive load change to resistive load

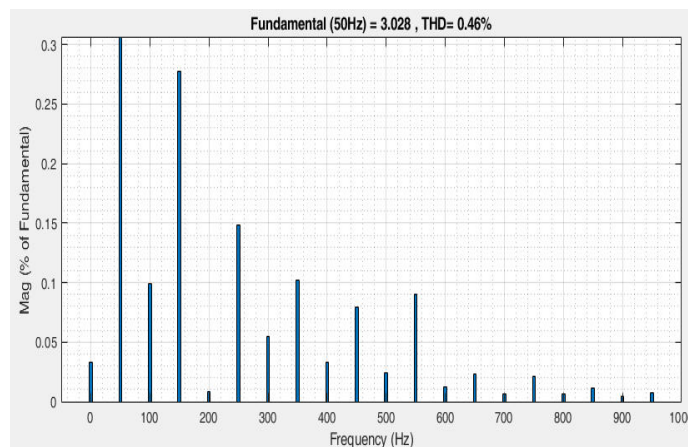
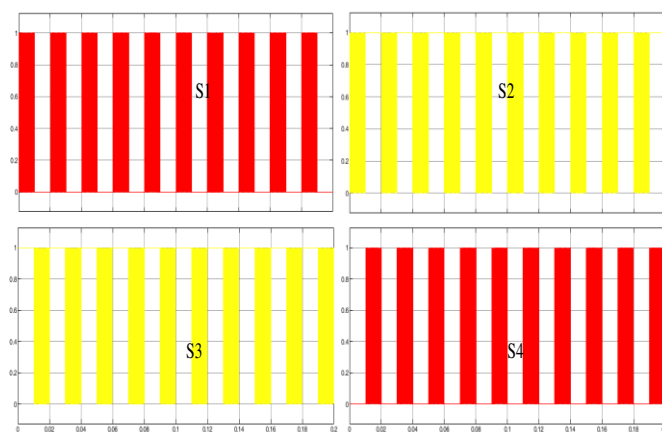


Figure 10: Total harmonic distortion (THD) profile of output current



(a)

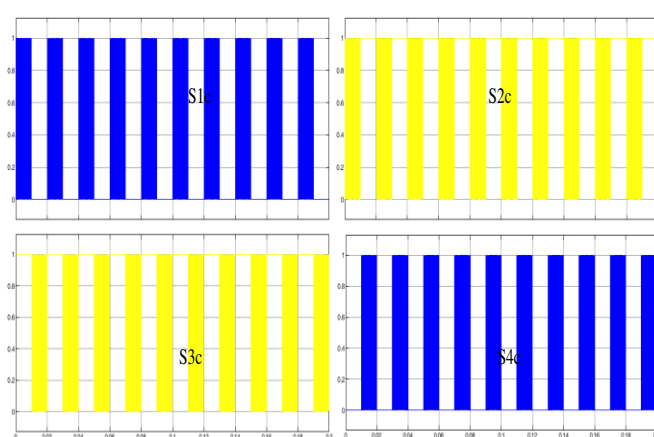


Figure 11: PWM switching gate signals

V. CONCLUSION

Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It should be noted that the lower switching frequency usually means lower switching loss and higher efficiency. Hence, switching and conduction losses of the proposed inverter will be very less when compared to the other type of topologies.

In this intense the inductive load change from 100Ohm 200mH to 50Ohm 100mH at the time of 0.5sec. It can be clearly seen that the output voltage has not change at this time but output current has been doubled at this point. Its changes from 1.5A to the 3A after doing half of the inductive load.

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